ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -18 (ANSWER KEY)

Topic – JK, Master-Slave, D and T flip flops

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 22/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. In J-K flip-flop, if J = 1 and K=0 the output is said to be _____
   a) **Set**
   b) Reset
   c) Previous state
   d) Current state
2. In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____
   a) D flip-flop
   b) S-R flip-flop
   c) **T flip-flop**
   d) S-K flip-flop
3. Both the J-K & the T flip-flop are derived from the basic _____
   a) S-R flip-flop
   b) **S-R latch**
   c) D latch
   d) D flip-flop
4. The flip-flops which has not any invalid states are _____
   a) S-R, J-K, D
   b) S-R, J-K, T
   c) J-K, D, S-R
   d) **J-K, D, T**
5. What does the triangle on the clock input of a J-K flip-flop mean?
   a) Level enabled
   b) **Edge triggered**
   c) Both Level enabled & Edge triggered
   d) Level triggered
6. What does the circle on the clock input of a J-K flip-flop mean?
   a) Level enabled
   b) Positive edge triggered
   c) **negative edge triggered**
   d) Level triggered

7. What does the direct line on the clock input of a J-K flip-flop mean?
   a) Level enabled
   b) Positive edge triggered
   c) negative edge triggered
   d) **Level triggered**
8. In a positive edge triggered JK flip flop, a low J and low K produces?
   a) High state
   b) Low state
   c) Toggle state
   d) **No Change State**
9. S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____
   a) OR Gate
   b) AND Gate
   c) **Inverter**
   d) Full Adder
10. When both the inputs J and K have a HIGH state, the flip-flop switches to
   a) set
   b) reset
   c) **complement state**
   d) undefined
11. In J-K flip-flop, if J = 0 and K=1 the output is said to be _____
   a) Set
   b) **Reset**
   c) Previous state
   d) Current state
12. The following flip-flop is used as latch:
   a) JK flip flop
   b) **D flip-flop**
   c) T flip-flop
   d) SR flip-flop
13. What kind of drawback of SR flip-flop is removed by JK flip-flop?
   a) S=0, R=0
   b) S=0, R=1
   c) S=1, R=0
   d) **S=1, R=1**
14. The output Q can be clocked low by setting JK input to:
   a) 1,1
   b) 1,0
   c) **0,1**
   d) 0,0

15. JK flip flop has
    a) temporary memory
    b) no memory
    c) **true memory**
    d) random memory

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