ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -22

Topic – Synchronous and asynchronous counters

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 26/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it.
   a. register
   b. memory unit
   c. flip-flop
   d. arithmetic logic unit
2. How many different states does a 3-bit asynchronous counter have?
   a. 2
   b. 4
   c. 8
   d. 16
3. A counter circuit is usually constructed of _____.
   a. A number of latches connected in cascade form
   b. A number of NAND gates connected in cascade form
   c. A number of flip-flops connected in cascade
   d. A number of NOR gates connected in cascade form
4. How many types of the counter are there?
   a. 2
   b. 3
   c. 4
   d. 5
5. A decimal counter has _____ states.
   a. 5
   b. 10
   c. 15
   d. 20
6. Ripple counters are also called _____.
   a. SSI counters
   b. Asynchronous counters
   c. Synchronous counters
   d. VLSI counters
7. The parallel outputs of a counter circuit represent the _____ .
   a. Parallel data word
   b. Clock frequency
   c. Counter modulus

d. Clock count

8. Normally, the synchronous counter is designed using _____
    a. S-R flip-flops
    b. J-K flip-flops
    c. D flip-flops
    d. T flip-flops
9. Synchronous counter is a type of _____.
    a. SSI counters
    b. LSI counters
    c. MSI counters
    d. VLSI counters
10. How many natural states will there be in a 4-bit ripple counter?
    a. 4
    b. 8
    c. 16
    d. 32
11. A ripple counter's speed is limited by the propagation delay of _____.
    a. Each flip-flop
    b. All flip-flops and gates
    c. The flip-flops only with gates
    d. Only circuit gates
12. Which type of triggering phenomenon is exhibited by Counters?
    a. Edge
    b. Level
    c. Pulse
    d. All of the above
13. The minimum number of flip-flops required to construct a mod 64(divisible by 64) ripple counter are:
    a. 4 flip-flops
    b. 8 flip-flops
    c. 16 flip-flops
    d. 64 flip-flops
14. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
    a. input clock pulses are applied only to the first and last stages
    b. input clock pulses are applied only to the last stage
    c. input clock pulses are not used to activate any of the counter stages
    d. input clock pulses are applied simultaneously to each stage
15. In digital logic, a counter is a device which _____.
    a. Counts the number of outputs
    b. Stores the number of times a particular event or process has occurred
    c. Stores the number of times a clock pulse rises and falls
    d. Counts the number of inputs

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