ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -23

Topic – Ripple & Decade Counter

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 27/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. A down counter using n-flip-flops count _____
   a) Downward from a maximum count
   b) Upward from a minimum count
   c) Downward from a minimum to maximum count
   d) Toggles between Up and Down count
2. Which of the following statements are true?
   a) Asynchronous events does not occur at the same time
   b) Asynchronous events are controlled by a clock
   c) Synchronous events does not need a clock to control them
   d) Only asynchronous events need a control clock
3. UP Counter is _____
   a) It counts in upward manner
   b) It count in down ward manner
   c) It counts in both the direction
   d) Toggles between Up and Down count
4. DOWN counter is _____
   a) It counts in upward manner
   b) It count in downward manner
   c) It counts in both the direction
   d) Toggles between Up and Down count
5. How many different states does a 3-bit asynchronous down counter have?
   a) 2
   b) 4
   c) 6
   d) 8
6. In a 3-bit asynchronous down counter, the initial content is _____
   a) 000
   b) 111
   c) 010
   d) 101
7. A ripple counter's speed is limited by the propagation delay of _____
   a) Each flip-flop
   b) All flip-flops and gates
   c) The flip-flops only with gates
   d) Only circuit gates

8. A principle regarding most display decoders is that when the correct input is present, the related output will switch _____
   a) HIGH
   b) To high impedance
   c) To an open
   d) LOW
9. Three decade counter would have _____
   a) 2 BCD counters
   b) 3 BCD counters
   c) 4 BCD counters
   d) 5 BCD counters
10. BCD counter is also known as _____
   a) Parallel counter
   b) Decade counter
   c) Synchronous counter
   d) VLSI counter
11. How many flip-flops are required to construct a decade counter?
   a) 4
   b) 8
   c) 5
   d) 10
12. What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs?
   a) The output increases by 1
   b) The output decreases by 1
   c) The output word increases by 2
   d) The output word decreases by 2
13. The output of UP counters goes on increasing due to _____.
   a) Transmission of clock pulses
   b) Reception of clock pulses
   c) Both a and b
   d) None of the above
14. How many flip-flops are required to construct a MOD-32 binary counter?
   a) 4
   b) 8
   c) 5
   d) 10

15. If the output of two-bit asynchronous binary up counter using T flip flops is '00' at reset condition, then what output will be generated after the fourth negative clock edge?

   a) 00
   b) 01
   c) 10
   d) 11

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