ST. LAWRENCE HIGH SCHOOL

FOR GOD AND COUNTRY

A Jesuit Christian Minority Institution

WORKSHEET -15(ANSWER KEY)

Topic – Introduction to Sequential Logic Circuits

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 18/06/2020**

Choose the correct answer for each question: 15x1=15

1. What is/are the crucial function/s of memory elements used in the sequential circuits?

   a. Storage of binary information

   b. Specify the state of sequential

   c. Both a & b

   d. None of the above

2. How are the sequential circuits specified in terms of time sequence?

   a. By Inputs

   b. By Outputs

   c. By Internal States

   d. All of the above

3. The behaviour of synchronous sequential circuit can be predicted by defining the signals at _____.

   a. discrete instants of time

   b. continuous instants of time

   c. sampling instants of time

   d. at any instant of time

4. The output of a sequential circuit depends on

a. Present inputs only

b. Past outputs only

c. **Both present and past inputs**

d. Present outputs only

5. The clock signals are used in sequential logic circuits to

a. Tell the time of the day

b. Tell how much time has elapsed since the system was turned on

c. Carry parallel data signals

d. **Synchronize events in various parts of system**

6. Synchronous Sequential circuits can be used in :

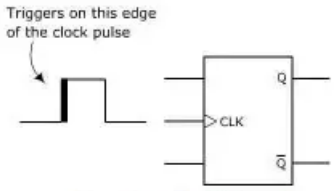
a. Synchronous counters

b. Flip-flops

c. **Both (a) and (b)**

d. None of these

7. The following diagram represents :



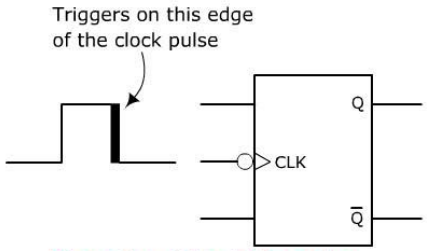
a. **Positive edge triggering**

b. Negative edge triggering

c. Level triggering

d. None of these

8. The following diagram represents:



a. Positive edge triggering

b. <u>Negative edge triggering</u>

c. Level triggering

d. None of these

9. _____ allows a circuit to become active at the positive or negative edge of the clock signal.

a. Positive level triggering

b. Negative level triggering

c. <u>Edge triggering</u>

d. None of these

10. In _____ , an event occurs during the high voltage or low voltage.

a. Positive edge triggering

b. Negative edge triggering

c. <u>Level triggering</u>

d. None of these

11. Flip-flops are:

a. Level-triggered

b. <u>Edge-triggered</u>

c. Both (a) and (b)

d. None of these

12. Latches are:

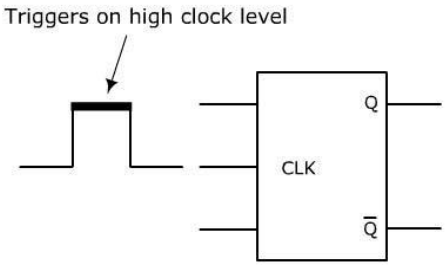
a. <u>Level-triggered</u>

b. Edge-triggered

c. Both (a) and (b)

d. None of these

13. The following diagram represents:



a. <u>Positive level triggering</u>

b. Negative level triggering

c. Edge triggering

d. None of these

14. _____acts as a memory element for one bit of data.

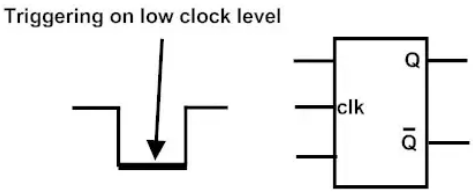
a. <u>Flip-flop</u>

b. Clock pulse

c. Input pulse

d. Output signal

15. The following diagram represents:



a. Positive level triggering

b. <u>Negative level triggering</u>

c. Edge triggering

d. None of these

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