ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -20

Topic – Flip-flops

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 24/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. What is the significant capacity of memory elements utilized in the sequential circuits?
    a. Storage of binary information
    b. Specify the state of sequential
    c. Both (a) and (b)
    d. State machine
2. The table that is not a part of the asynchronous analysis procedure:
    a. Transition table
    b. State table
    c. Flow table
    d. Excitation table
3. Asynchronous circuits are useful in application where the input signals may:
    a. Change at any time
    b. Never change
    c. Both (a) and (b)
    d. Continuously change
4. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____
    a. SET
    b. RESET
    c. Clear
    d. Invalid
5. The SR latch consists of:
    a. 1 input
    b. 2 inputs
    c. 3 inputs
    d. 4 inputs
6. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature:
    a. Low input voltages
    b. Synchronous operation
    c. Gate impedance
    d. Cross coupling
7. The logic circuits whose outputs at any instant of time depend only on the present input but also on the past outputs are called _____.
    a. Combinational circuits

b. Sequential circuits
c. Latches
d. Flip-flops

8. The basic latch consists of _____.
    a. Two inverters
    b. Two comparators
    c. Two amplifiers
    d. Two adders
9. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
    a. Because of inverted outputs
    b. Because of triggering functionality
    c. Because of cross-coupled connection
    d. Because of inverted outputs & triggering functionality
10. What is one disadvantage of an S-R flip-flop?
    a. It has no Enable input
    b. It has a RACE condition
    c. It has no clock input
    d. Invalid State
11. What is a trigger pulse?
    a. A pulse that starts a cycle of operation
    b. A pulse that reverses the cycle of operation
    c. A pulse that prevents a cycle of operation
    d. A pulse that enhances a cycle of operation
12. Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?
    a. S=R=0
    b. S=0, R=1
    c. S=1, R=0
    d. S=R=1
13. A flip-flop changes its state during the:
    a. complete operational cycle
    b. falling edge of the clock pulse
    c. rising edge of the clock pulse
    d. both answers (b) and (c)
14. In S-R flip-flop, if Q = 0 the output is said to be _____
    a. Set
    b. Reset
    c. Previous state
    d. Current state
15. The purpose of the clock input to a flip-flop is to:
    a. clear the device
    b. set the device
    c. always cause the output to change states
    d. cause the output to assume a state dependent on the controlling (J-K or D) inputs.

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