ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -17 (ANSWER KEY)

Topic – SR Flip-flop

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 20/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called:
   a) Combinational circuits
   b) **Sequential circuits**
   c) Latches
   d) Flip-flops
2. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
   a) AND or OR gates
   b) XOR or XNOR gates
   c) **NOR or NAND gates**
   d) AND or NOR gates
3. How many VALID entries of the truth table for an S-R flip-flop have?
   a) 1
   b) 2
   c) 3
   d) 4
4. Latch together with a triggering circuit form a:
   a) inductor
   b) **flip-flop**
   c) timing generator
   d) sine generator
5. One example of the use of an S-R flip-flop is as _____
   a) Transition pulse generator
   b) Racer
   c) **Switch debouncer**
   d) Astable oscillator
6. How many NAND gates are required to construct SR flip flop?
   a) four
   b) three
   c) **two**
   d) one

7. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
   a) AND or OR gates
   b) XOR or XNOR gates
   c) **NOR or NAND gates**
   d) AND or NOR gates
8. In S-R flip-flop, if Q = 0 the output is said to be _____
   a) Set
   b) **Reset**
   c) Previous state
   d) Current state
9. When set input of a S-R flip-flop is high and R=0, the output will _____
   a) Be invalid
   b) Change
   c) Not change
   d) **high**
10. Which state is undefined in SR flip-flop?
   a) S=0, R=0
   b) S=0, R=1
   c) S=1, R=0
   d) **S=1, R=1**
11. Race condition occurs in:
   a) Synchronous
   b) **Asynchronous**
   c) Combinational
   d) All of the above
12. The full form of SR in SR flip-flop is _____
   a) System rated
   b) **Set reset**
   c) Set ready
   d) Set Rated
13. It is present in flip-flop, but absent in latch:
   a) input state
   b) output state
   c) inverter
   d) **clock**
14. What is the output of SR flip-flop for the following input: S=0 and R=0?
   a) set
   b) **reset**
   c) undefined
   d) unchanged

15. One major difference between a NAND based S'-R' latch & a NOR based S-R latch is :
    a) **The inputs of NOR latch are 0 but 1 for NAND latch**
    b) The inputs of NOR latch are 1 but 0 for NAND latch
    c) The output of NAND latch becomes set if S'=0 & R'=1 and vice versa for NOR latch
    d) The output of NOR latch is 1 but 0 for NAND latch

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