ST. LAWRENCE HIGH SCHOOL

A Jesuit Christian Minority Institution

FOR GOD AND COUNTRY

WORKSHEET -16

Topic – Latches

Subject: COMPUTER SCIENCE **Class - 12** **F.M:15**

Chapter: Sequential Logic Circuits **Date: 19/06/2020**

Choose the correct answer for each question: [15 X 1 = 15]

1. A latch is an example of a _____
   a) Monostable multivibrator
   b) Astable multivibrator
   c) Bistable multivibrator
   d) 555 timer
2. Latch is a :
   a) Synchronous device
   b) Asynchronous device
   c) both (a) and (b)
   d) none of these
3. Latch is a device with _____
   a) One stable state
   b) Two stable state
   c) Three stable state
   d) Infinite stable states
4. Latches consist of
   a) inductors
   b) inverters
   c) timing generators
   d) frequency generators
5. Latch does not contains:
   a) input state
   b) output state
   c) inverter
   d) clock
6. Why latches are called memory devices?
   a) It has capability to stare 8 bits of data
   b) It has internal memory of 4 bit
   c) It can store one bit of data
   d) It can store infinite amount of data

7. Latches are basic storage elements that operate with
   a) signal levels
   b) signal transitions
   c) both (a) and (b)
   d) none of these
8. Two stable states of latches are _____
   a) Astable & Monostable
   b) Low input & high output
   c) High output & low output
   d) Low output & high input
9. Which of the following is **NOT** a type of latch?
   a) SR latch
   b) DJ latch
   c) JK latch
   d) T latch
10. The full form of SR is _____
   a) System rated
   b) Set reset
   c) Set ready
   d) Set Rated
11. The SR latch consists of _____
   a) 1 input
   b) 2 inputs
   c) 3 inputs
   d) 4 inputs
12. The outputs of SR latch are _____
   a) x and y
   b) a and b
   c) s and r
   d) q and q'
13. When both inputs of SR latches are low, the latch _____
   a) Q output goes high
   b) Q' output goes high
   c) It remains in its previously set or reset state
   d) it goes to its next set or reset state
14. When a high is applied to the Set line of an SR latch, then _____
   a) Q output goes high
   b) Q' output goes high
   c) Q output goes low
   d) Both Q and Q' go high

15. Which of the following state is illegal or invalid?
    a) S=0 and R=0
    b) S=0 and R=1
    c) S=1 and R=0
    d) S=1 and R=1

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